IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) A shift register circuit, comprising:

a data input;

a plurality of stages, each comprising a data latch circuit for storing a bit of data, a pointer latch circuit for storing a bit of pointer information;

transfer circuitry for serially transferring bits of data presented at the data input and to be stored in the data latch circuits through the plurality of stages during a first mode of operation; and

pointer advance circuitry for serially transferring one or more bits of pointer information forming a pointer through the plurality of stages during a second mode of operation without disturbing bits of data stored in the data latch circuits.

2. (Currently Amended) The shift register circuit of claim 1, wherein the pointer indicates ~~, as selected,~~ a stage having a pointer latch circuit storing a bit of a different logic level than a bit stored in a pointer latch circuit of a preceding stage.

3. (Original) The shift register circuit of claim 1, wherein the pointer advance circuitry comprises, for each stage, a switched reset path between a first node of a pointer latch circuit and ground.

4. (Original) The shift register circuit of claim 3, wherein the pointer advance circuitry is configured to advance a bit of pointer information from a first stage to a subsequent stage by closing the reset path.

5. (Original) The shift register circuit of claim 4, wherein the switched reset path comprises at least two serially connected transistors, each responsive to a bit of pointer information stored in a pointer latch circuit of a different stage.

6. (Original) The shift register circuit of claim 1, further comprising circuitry for presetting the bit of pointer information stored in each pointer latch circuit.

7. (Original) The shift register circuit of claim 1, wherein the pointer advance circuitry is configured to asynchronously advance the pointer.

8. (Original) The shift register circuit of claim 1, wherein the transfer circuitry comprises first transfer switches coupled between fuse latch circuits and data latch circuits of adjacent stages and second transfer switches coupled between fuse latch circuits and data latch circuits of the same stage, wherein the first transfer circuits are responsive to a first clock signal and the second transfer circuits are responsive to a second clock signal.

9. (Original) The shift register of claim 8, wherein the first and second clock signals are operating in a complementary manner during the first mode of operation and held at the same logic level during the second mode of operation.

10. (Currently Amended) A fuse programming circuit for sequentially programming a plurality of fuses, comprising:

a shift register having:

a plurality of stages, each comprising a fuse latch circuits for holding fuse programming data indicating which of the fuses are to be blown, and a pointer latch circuit ~~a plurality of pointer latch circuits~~ for holding bits of a pointer for selecting one of the fuses, and

a pointer advance circuitry for serially advancing the pointer to select different fuses without disturbing bits of data stored in the data latch circuits; and

one or more blow circuits configured to apply a blow voltage to a fuse selected by the pointer if the fuse programming data stored in a corresponding fuse latch circuit indicates the selected fuse is to be blown.

11. (Original) The fuse programming circuit of claim 10, wherein the one or more blow circuits are configured to apply the blow voltage to a fuse selected by pointer if the fuse programming data stored in a corresponding fuse latch circuit indicates the selected fuse is to be blown synchronized with a blow clock signal.

12. (Original) The fuse programming circuit of claim 10, wherein the pointer selects a fuse when a pointer latch circuit associated with the fuse contains a bit of a first logic level and a fuse pointer latch associated with a previously selected fuse contains a bit of a second complementary logic level.

13. (Original) The fuse programming circuit of claim 10, wherein the pointer advance circuitry is configured to advance the pointer only when a pointer advance signal is asserted.

14. (Original) The fuse programming circuit of claim 10, wherein the pointer advance circuitry is configured to advance the pointer only when a bit in a fuse latch circuit corresponding to a currently selected fuse is at a predetermined logic level.

15. (Original) The fuse programming circuit of claim 10, further comprising fuse latch reset circuitry configured to place the bit in the fuse latch circuit corresponding to the currently selected fuse to the predetermined logic level after the selected fuse has been programmed.

16. (Original) A method for maintaining both pointer and data information in a shift register having multiple stages, each stage having a pointer latch circuit and a fuse latch circuit, the method comprising:

shifting data bits into the data latch circuits through the pointer latch circuits;

decoupling the data latch circuits and pointer latch circuits;

initializing a pointer formed by bits stored in the pointer latch circuits to select a first stage of the shift register; and

serially advancing the pointer to select a second stage of the shift register by changing one or more bits stored in the pointer latch circuits without disturbing the data bits in the data latch circuits.

17. (Original) The method of claim 16, wherein:

initializing the pointer comprises storing a bit of a first logic level in a first pointer latch circuit and storing bits of a second logic level in the other pointer latch circuits; and

serially advancing the pointer comprises shifting the bit of the first logic level from the first pointer latch circuit to a second pointer latch circuit.

18. (Original) The method of claim 17, wherein serially advancing the pointer comprises providing a reset path between a node of the first pointer latch circuit and ground.

19. (Original) The method of claim 16, wherein serially advancing the pointer comprises asynchronously advancing the pointer.

20. (Original) The method of claim 19, wherein asynchronously advancing the pointer comprises advancing the pointer during a pointer advance mode defined by a clock signal until a stage having a data latch circuit storing a bit of a first logic level is selected.

21. (Currently Amended) A method for sequentially programming a plurality of fuses, comprising:

(a) loading a shift register having a plurality of stages with fuse programming data, wherein each stage of the shift register comprises a pointer latch circuit and a data latch circuit and each data latch circuit is configured to store a bit of fuse programming data to indicate whether an associated one of the fuses is to be blown;

(b) initializing a fuse pointer, formed by bits stored in the pointer latch circuits, to select a fuse;

(c) blowing the fuse selected by the fuse pointer if the bit of fuse programming data stored in the associated data latch circuit indicates the fuse is to be blown[[,]];

(d) advancing the pointer to select a subsequent fuse[[,]]; and

(e) repeating steps (c)-(d) until each of the fuses to be blown, as indicated by the respective bit of the fuse programming data, have been blown.

22. (Original) The method of claim 21, wherein initializing the fuse pointer comprises:

storing a bit of a first logic level in each of the pointer latch circuits; and

storing a bit of a second logic level in one of the pointer latch circuits.

23. (Original) The method of claim 21, wherein advancing the pointer comprises providing a reset path between a node of a pointer latch circuit and ground.

24. (Original) The method of claim 23, wherein providing a reset path comprises:

switching a first transistor receiving, as input, a logic level stored in a first pointer latch circuit; and

switching a second transistor receiving, as input, a logic level stored in a second pointer latch circuit.